The Virtual Packaging Laboratory

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Abstract

A key aspect of the student training process at the Packaging Research Center at the Georgia Institute of Technology is to provide students with hands-on "design, build, and operate" educational opportunities which reach beyond traditional classroom learning. The has developed a hands-on instructional laboratory that provides students with exposure to basic packaging substrate fabrication concepts and techniques, including interconnect design, dielectric deposition, via formation, metallization, and testing. This paper presents progress toward a plan to augment the hands-on packaging instructional laboratory with multimedia presentations and other advanced instructional support technology. The overall vision is to develop a virtual packaging laboratory in which a student can sit at a multimedia computer or workstation (equipped with the necessary audio, video and graphics capability) and follow a substrate through a simple processing sequence. To make this courseware remotely available for potential distance learning applications, it has been developed to be compatible with World-Wide Web access.

1. Introduction

The electronic products of the twenty-first century, from cellular phones to personal digital assistants to multimedia and network computers, are changing the way the world interacts and communicates. These products result from the revolutionary progress underway in computers, automotive technology, telecommunications and consumer electronics. The commonality between these commodities and the services they provide is the need for low-cost, high-performance electronics. Toward this end, the Packaging Research Center (PRC) at the Georgia Institute of Technology is engaged in developing packaging technologies for the future, primarily utilizing multichip module (MCM) technology as a focal point. In addition to performing basic and applied research, as an academic institution, the PRC has the parallel responsibility to educate and train students to meet the needs of industry. The PRC has enthusiastically accepted this challenge and constantly seeks ways to better prepare students to be competitive packaging engineers in a global marketplace.

Theoretical information on concepts relevant to package fabrication is typically covered by a variety of courses in the Electrical Engineering, Chemical Engineering, Materials Science and Physics curricula. To enhance this classroom education, the PRC has developed a hands-on instructional electronics packaging laboratory designed to provide students with a practical experience in packaging substrate processing. This "design, build and operate" (DBO) educational opportunity is necessary to provide students with design and fabrication skills. This hands-on laboratory includes instruction in basic processing concepts and techniques, including interconnect design, dielectric deposition, via formation, metallization and interconnect testing.

In general, space, equipment and/or budget constraints often limit the opportunity for DBO-like educational opportunities. For example, the Georgia Tech Microelectronics Research Center has developed a laboratory course for the fabrication of ICs at the initial cost of over $1M and an ongoing annual cost of approximately $50K. This exorbitant expense is a principle factor in why many universities, especially those that do not focus on engineering, fail to offer these types of courses to their students. Opportunities to fabricate packaging substrates in an educational setting are rare, despite the high industry demand for skilled engineers and serious student interest.

In order to enhance the educational experience of students enrolled in the hands-on laboratory, with funding from NSF and IEEE, we have developed a virtual electronics packaging laboratory that is compatible with the World-Wide Web [1]. This web site allows a student, with access to a high-performance multimedia workstation containing the necessary audio, video and graphics capabilities, to follow a substrate through a simple processing sequence. This virtual packaging laboratory can be viewed using web browsers such as *Netscape Navigator* and Microsoft's *Internet Explorer*, making this web site remotely available for potential distance learning applications.

2. Substrate Fabrication Process

MCMs are classified as either laminated (MCM-L), ceramic (MCM-C), or deposited (MCM-D), depending on the substrate technology [2]. To optimize cost and performance tradeoffs in MCM technologies, the high performance of MCM-D at the relatively low cost of MCM-L is desirable. This hybrid technology is called MCM-L/D. In this MCM technology, the substrate structures are formed as multiple layers of metal separated by dielectric material. Figure 1 is an example of the PRC's single-level integrated module (SLIM) implementation of the MCM-L/D paradigm.

The fabrication process for SLIM substrates consists of a series of diverse steps, including dielectric deposition, via formation and metallization. In the hands-on laboratory course that serves as the foundation for the Virtual Packaging Laboratory simulation environment, students progress through an approximately twelve-week sequence in which the process steps are taught by a professor in a lecture and performed by the students in the laboratory.

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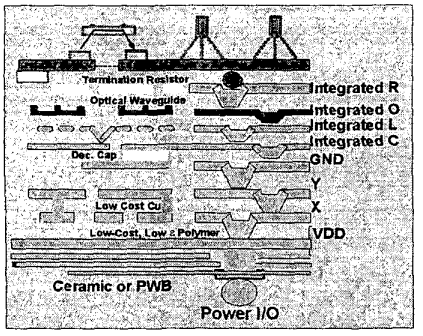

Figure 1 - Single-level integrated module (SLIM) implementation of an MCM-L/D substrate.

The Virtual Packaging Lab website presents the packaging steps in the following sequence:

- Dielectric deposition
- Pre-bake
- Exposure
- Development
- Cure
- Plasma De-scum
- Metallization

Dielectric deposition is the first step in the substrate fabrication process. There are many different techniques used to coat the substrate with a dielectric. Spin coating and meniscus coating are the techniques covered in the laboratory and on the web site. In spin coating, the dielectric is spread across the substrate by rotational forces. In meniscus coating, the substrate is coated using an applicator tube through which the dielectric material is pumped. Once the substrate has been coated, it is baked for a short period of time. This is known as the pre-bake step. Pre-baking causes thermally induced reactions to occur creating a temporary adhesion of the dielectric to the substrate.

The exposure and development steps form vias in the photosensitive dielectric. During exposure, UV light is used to pattern the substrate through a mask, transferring the via patterns. In the subsequent development step, the exposed pattern is removed from the substrate, thus forming vias. Next, curing necessary to stabilize the substrate. The cured substrate then undergoes a plasma de-scum procedure, the objective of which is to clean residue at the bottom of the vias. Metallization is the final step in covered in substrate fabrication. During metallization, a layer of copper is deposited on the substrate surface to fill vias and provide electrical contact between devices. Because of the diversity techniques used in industry, the Virtual Packaging Lab describes alternate methods for performing some of the above procedures, and compares and contrasts all available techniques. For example, the web site includes both spin coating and meniscus coating as dielectric deposition techniques. In addition, the metallization pages cover both electroless and electrolytic plating.

In addition to the unit processes mentioned above, the lab course also includes sections on lab safety, interconnect design, and interconnect testing. Eventually, each of these topics will also be included in the Virtual Packaging Lab web site (see Section 4 below).

3. Virtual Packaging Laboratory Operation

The Virtual Packaging Laboratory uses hypertext markup language (HTML) frame programming to create interdependent modules of information. These modules are joined through hyperlinks embedded into the HTML frame syntax. Text, graphics, video, Java applets, and simulation software are all utilized to convey information to the user. Package substrate fabrication is demonstrated through navigation, with the aid of a mouse, of the embedded hyperlinks that exist on the site.

The fabrication procedures and theory are accessed three ways: (1) through a "Process Steps" menu, which includes a graphical flow table; (2) by selecting from a process steps/theory "Main Menu"; and (3) by clicking the mouse on the equipment the user wishes to see demonstrated from a graphical map layout of physical laboratory. In addition, each process step page for a particular piece of equipment and corresponding process theory are interconnected via hyperlinks present in the graphical logo present on all process step/theory pages. At the highest level, the users have access to the following selections: a process flow chart, process steps and theory menus, interconnect design, interconnect testing, lab environment (which includes lab safety and the laboratory map), a glossary, related links, the site layout, the mission statement, the authors, and the welcome page as shown in Figure 2.

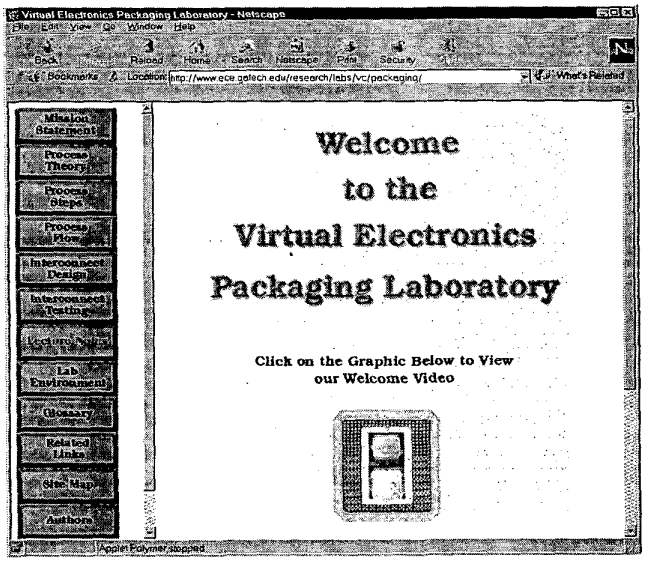

Figure 2 - Virtual Packaging Laboratory home page.

3.1. Welcome Video

The welcome page of the website includes a package graphic that when clicked on instantiates an mpeg stream video. This video can be viewed by any of the media players that come with today's common operating systems such as Microsoft NT/98, Unix and Macintosh. The purpose of this video is to welcome the new user to the Virtual Packaging Laboratory by putting a face and voice to the website's

creators. Included in the video is an exterior and interior visual of the Georgia Tech Manufacturing Research Center (where the physical laboratory is located), information about the webites purpose and acknowledgement of the funding provided by the NSF and IEEE. The PRC is also introduced as a sponsor of the hands-on laboratory.

3.2. Interconnect Design

Interconnect design was one of the first modules listed when this web site was envisioned. Interconnect design is obviously a major issue in packaging substrate fabrication. Recent processing advances allow thinner interconnect lines to be produced with smaller spaces that result in signal propagation, timing, and cross-talk issues. The interconnect design module contains the information necessary to help students address these issues.

3.3. Process Steps

Each fabrication step has an HTML module detailing the piece of equipment used to accomplish the desired process and instructions for its use. The basic modules included are: dielectric deposition, pre-bake, photolithography, curing, plasma de-scumming, and metallization. In addition, the dielectric deposition module contains hyperlinks to spin coating and meniscus coating, while the photolithography module allows access to the exposure and development processes. These pages are interconnected by means of a side menu embedded within HTML frame code, as well as hyperlinks present in the graphical logo at the top of each page. HTML frame code splits the monitor screen in to two sections so that the user can have access to a menu on the left hand side and information on the right. This coding provides for ease of movement within the web site. A majority of information present is conveyed to the user through text and graphics as demonstrated in Figure 3 below.

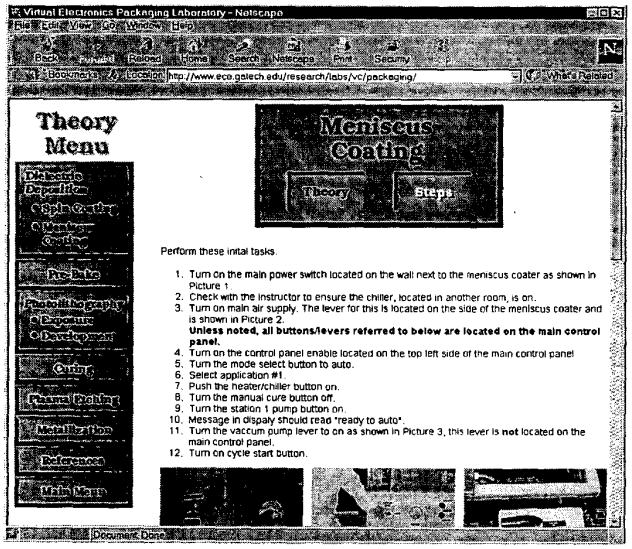

Figure 3. Meniscus Coating Steps Page.

3.4. Process Theory

There are three ways for a student to access the process theory related to a given procedure: (1) through hyperlinks present in the graphical logo at the top of the process step page; (2) by accessing the process theory button present when a student first enters the web site; and (3) by accessing the site map which provides a link to either the process theory menu or by directly clicking on the desired theory section. Theory sections are generally text explanations that can also include equations, figures and comparison charts. Within the text presented for a process, there are hyperlinks that lead to other areas of the site, which explain a particular concept or term in more detail. A sample of a page from the theory section is shown in Figure 4.

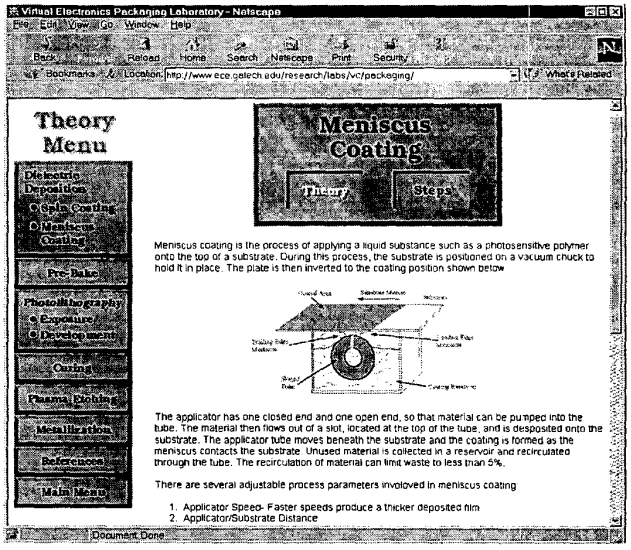

Figure 4. Meniscus Coating Theory Page.

3.5. Process Simulation: Java applet

The Virtual Packaging Laboratory currently contains one process simulation in the form of a Java applet. This applet was created to simulate the photolithography process using a graphical image of a piece of substrate coated with photosensitive polymer surmounted by a mask and light source. The user has control over how much energy is applied, the thickness in um of the polymer, and whether it is a negative or positive tone polymer. Once this information has been entered, the user views the results of the exposure and development process on the polymer. The user also has the ability to dynamically view the rate of change of the exposed feature by changing energy values using a scroll bar. Clicking on a link embedded in the photolithography theory page allows the student access to this applet. Figure 5 is a static representation of this applet.

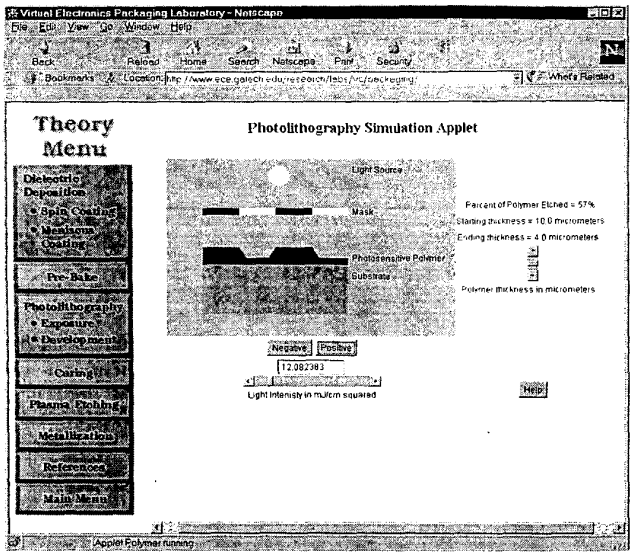

Figure 5. Static view of the Photolithography Applet.

3.6 Lecture Notes

The most recent addition to the web site is the inclusion of the information presented by the instructor in the hands-on laboratory lecture period. The presence of these notes on the website allows the students to prepare for lecture periods prior to attendance. This advance preparation facilitates a better understanding of the material being presented during class time and therefor a better understanding of the packaging fabrication process.

4. Future Plans

The design and creation of an interactive web site is an ongoing process. While much has been accomplished toward making the Virtual Packaging Laboratory a reality, there is still work to be done. Some information determined necessary at the project's inception still has yet to be included.

4.1. Interconnect Testing

Included in the Virtual Packaging Laboratory's initial specifications was a module on interconnect testing. Today's student must be familiar with testing techniques. Optimizing the production and fabrication of packaging substrates is essential in today's globally competitive market. This test module will provide information on the tools used to test substrates and the theory behind their use.

4.2. Integration of PROLITH Software

PROLITH is a software package used to aid in evaluating photolithography processes. We have acquired a demonstration version of this package and plan to interface the program to the web site via a Perl script [3]. An HTML page present on the web site will allow access to this script. This process simulator will provide direct feedback via simulated images of the consequences of various photolithography sequences on the via formation process.

5. Educational Benefits

The greatest motivation for the development of the Virtual Packaging Lab is the educational benefits the web site provides. The Virtual Packaging Lab serves primarily to augment the hands-on electronics packaging laboratory developed by the PRC. Since clean room access time is often limited, students enrolled in the course can prepare for a lab by using the web site to review procedure steps and theory. The Virtual Packaging Lab is based on the idea that learning can be nonlinear in nature. Students accessing the site can learn about and simulate different steps of the packaging process at their own pace.

The Virtual Packaging Lab will also benefit students not enrolled in the hands-on lab in a variety of ways. By providing background information and explanations of process steps, the web site will aid in the recruitment of students, not only for the packaging lab, but also for electronics packaging as a field of study. Because the Virtual Packaging Lab is accessible from the World-Wide Web, it is potentially available for distance learning. The web site will therefore be accessible to professionals as well as students at other schools.

6. Conclusion

Multimedia and hypermedia products are readily available today and continue to have a growing impact on education. The Virtual Packaging Laboratory (*http://www.ece.gatech.edu/research/labs/vc/packaging*) is designed to take advantage of their increasing popularity and ease of use to teach electronic packaging substrate fabrication techniques. It has been suggested by Neilsen that there are five criteria for evaluating hypermedia systems: 1) ease of learning; 2) ease of use; 3) ease of remembering of how to use; 4) minimal errors; and 5) pleasantness of use [4]. We believe that this web site amply meets these guidelines and with continuing improvements will surpass its present design.

Acknowledgement

The authors wish to thank IEEE and the National Science Foundation (Grant No. EEC-9402723) for support of this research.

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